Pre-Lab 3

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**Problem 1. Adder IC (74LS283)**

The mathematical equation computed by the 4-bit adder is

Cin+ 20(A0+B0) + 21(A1+B1) + 22(A2+B2) + 23(A3+B3) = 20S0 + 21S1 +22S2 + 23S3 + 24Cout.

* 1. Pin 16 is VCC.
  2. Pin 8 is GND.
  3. For input A (same for B and output S), A3 is the more significant bit.
  4. Compute 8 + 12 using the binary adder using the binary adder logic symbol. Draw an image of the logic symbol and label the appropriate inputs and outputs with a 1 or a 0.

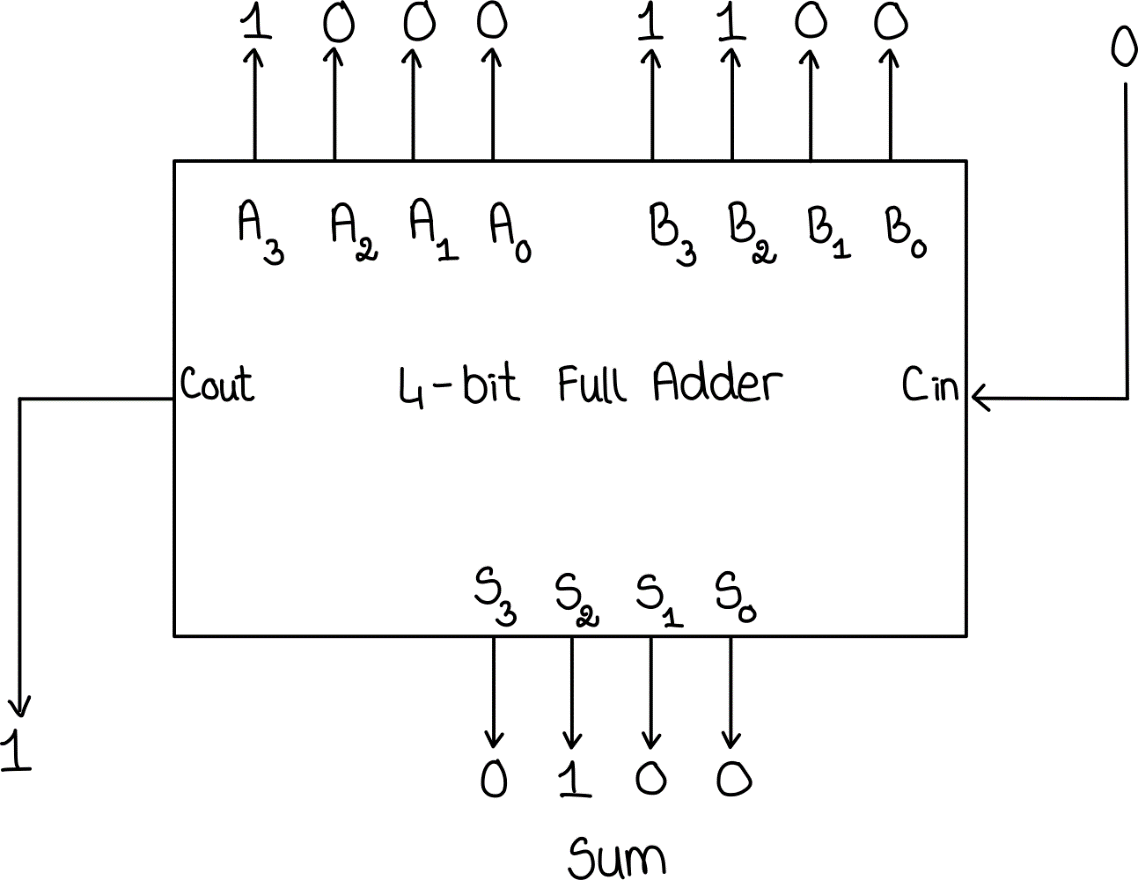
Cin = 0

A = 8 = 10002

B = 12 = 11002

S = 01002

Cout = 1 (Overflow)



* 1. Compute 5 + 6 using the binary adder IC pinout. Draw an image of the IC chip and label the appropriate pins with a 1 and 0. Include VCC and GND.

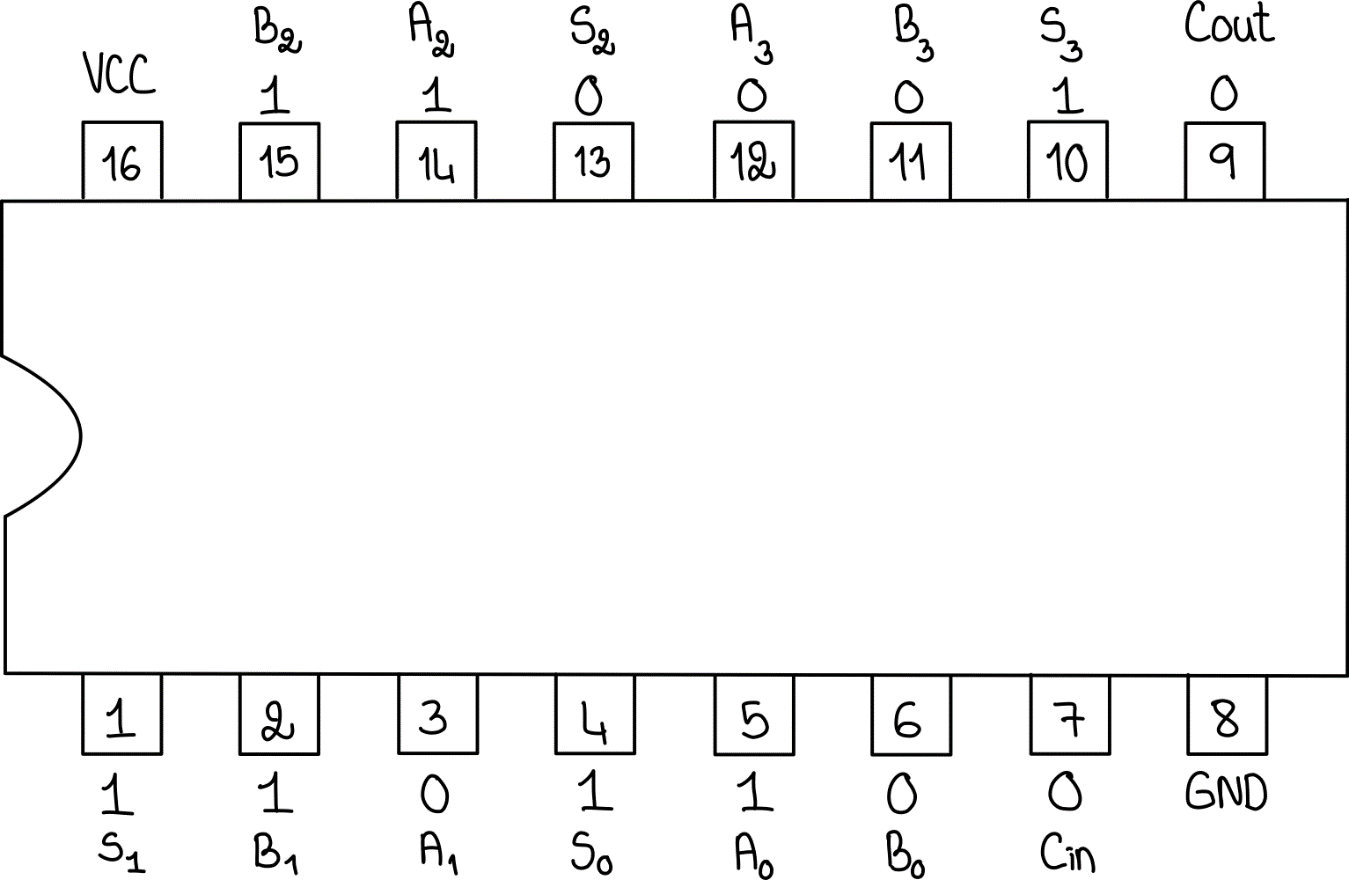
Cin = 0

A = 5 = 01012

B = 6 = 01102

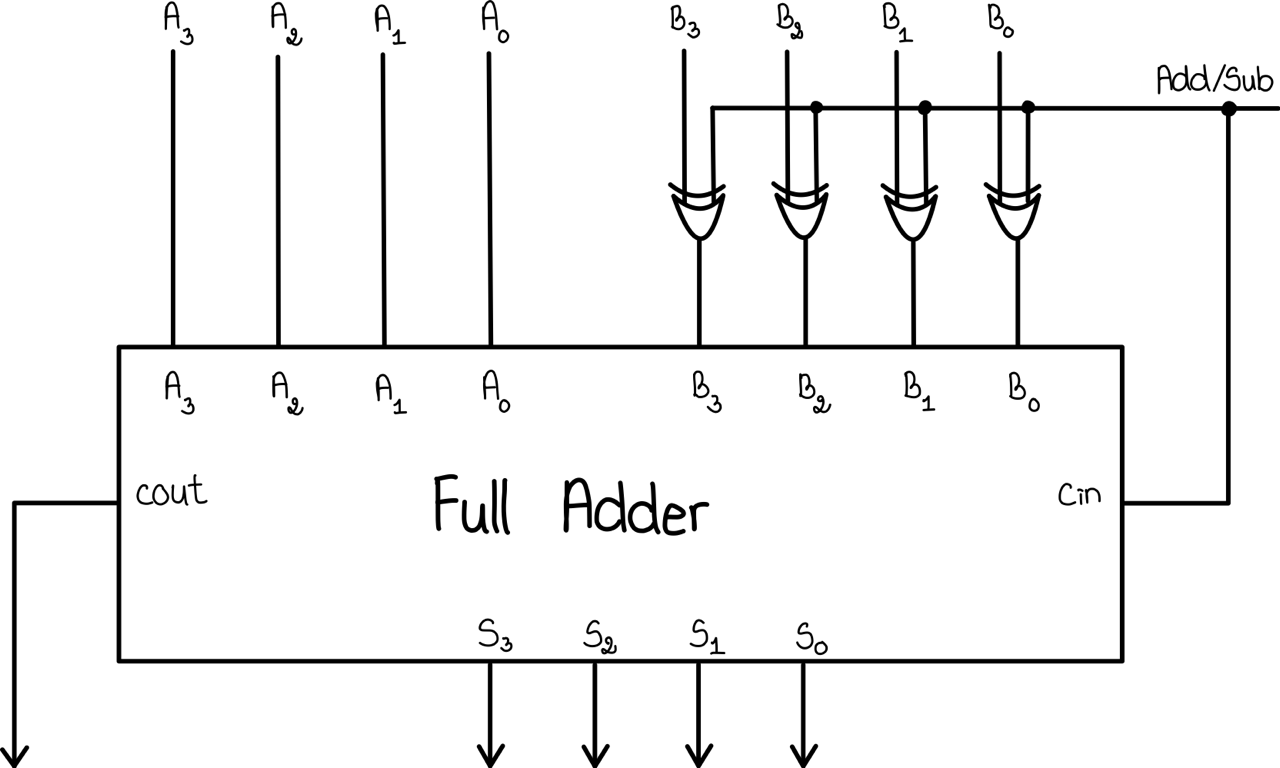
S = 10112

Cout = 0 (No Overflow)



**Problem 2. Subtraction with Two’s Complement**

1. To manipulate the bits of B to do both add and subtract is by using XOR gate between Cin and B. If Cin=0 or the remain is the same, then it does addition. If Cin=1 or all B’s bits are flipped, then it does subtraction.
2. Draw the logic diagram (not circuit diagram) of the 4-bit adder/subtractor. For the Full Adder, use the logic symbol in the first page. A logical diagram should contain block notations (such as Full Adder, D Flip-Flop, Decoder, Multiplexer) and gate symbols (such as AND, OR, and NOT).



**Problem 3. 1-Digit BCD Full Adder**

Learn about Binary Coded Decimal. Check the logic behind a 1-digit BCD full adder. Come up with a truth table and logic diagram for the BCD full adder. (Note : You have to implement the same question in the lab). A logical diagram should contain block notations (such as Full Adder, D Flip-Flop, Decoder, Multiplexer) and gate symbols (such as AND, OR, and NOT).

**Truth Table**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Decimal | Binary Sum | | | | | BCD Sum | | | | |
| K | Z8 | Z4 | Z2 | Z1 | C | S8 | S4 | S2 | S1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 13 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 15 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 16 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |

**Logic Diagram**

